Chapter - 5

Results and analysis

5.1 Introduction

This chapter provides the results of each simulation carried out as per the detailed simulation criteria mentioned in the previous chapter. The results are provided in this chapter as the same sequence of simulations carried out as per the Table 4.3 and Table 4.4.

The results of each simulation are given by an output data file which contains a set of binary values giving the occurrence of back flashover events for each simulation run. The binary value "0" means an occurrence of a back flashover event whereas "1" gives the negation of that event. A typical view of an output data file is shown in the Figure 5.1. As shown in the figure 5.1, the columns MBRK11, MBRK12 and MBRK13 gives the back flashover events occurred on TOP, MIDDLE and BOTTOM phases of circuit-1 of Tower-M respectively. Similarly the columns MBRK21, MBRK22and MBRK23 gives the back flashover events occurred on TOP, MIDDLE

Optimization Output Viewer - [towerL1areesters2ohm62]

Multiple Run Output File

Run #	x	Ph	Rf	MBRK11	MBRK12	MBRK13...	MBRK21...	MBRK22...	MBRK23
1	30	0	62	1	1	1	1	1	1
2	40	0	62	1	1	1	1	1	1
3	50	0	62	1	1	1	1	1	1
4	60	0	62	1	1	1	1	1	1
5	70	0	62	0	1	1	1	1	1
6	80	0	62	0	1	1	1	1	1
7	90	0	62	0	1	1	1	1	1
8	100	0	62	0	1	1	1	1	1
9	110	0	62	0	1	1	1	1	1
10	120	0	62	0	0	1	1	0	1
11	130	0	62	0	1	1	1	1	1
12	140	0	62	0	0	1	1	0	1
13	150	0	62	0	0	1	1	0	1
14	160	0	62	0	0	1	1	0	1
15	170	0	62	0	0	1	1	0	1
16	180	0	62	0	0	1	0	0	1
17	190	0	62	0	0	1	0	0	1
18	200	0	62	0	0	1	0	0	1
19	30	10	62	1	1	1	1	1	1
20	40	10	62	1	1	1	1	1	1
21	50	10	62	1	1	1	1	1	1
22	60	10	62	1	1	1	1	1	1
23	70	10	62	0	1	1	1	1	1
24	80	10	62	0	1	1	1	1	1
25	90	10	62	0	1	1	1	1	1
26	100	10	62	0	1	1	1	1	1
27	110	10	62	0	1	1	1	1	1
28	120	10	62	0	0	1	1	0	1
29	130	10	62	0	0	1	1	0	1
30	140	10	62	0	0	1	1	0	1

Figure 5.1 – Typical view of an output data file

and BOTTOM phases of circuit-2 of Tower-M respectively.

Based on the information provided by the output files of each simulation; the variation of minimum current required for back flashover event were plotted and are produced here as the final results.

5.2 Back flashover minimum current variation results and analysis

5.2.1 Results of simulations without arrester protection (Step-1)

The step-1 consists of six numbers of simulations from simulation no-01 to 06. All these six numbers of simulations were carried out without arrester module for both 8x20μs and 1.2x50μs surge waveforms respectively. Further above simulations were

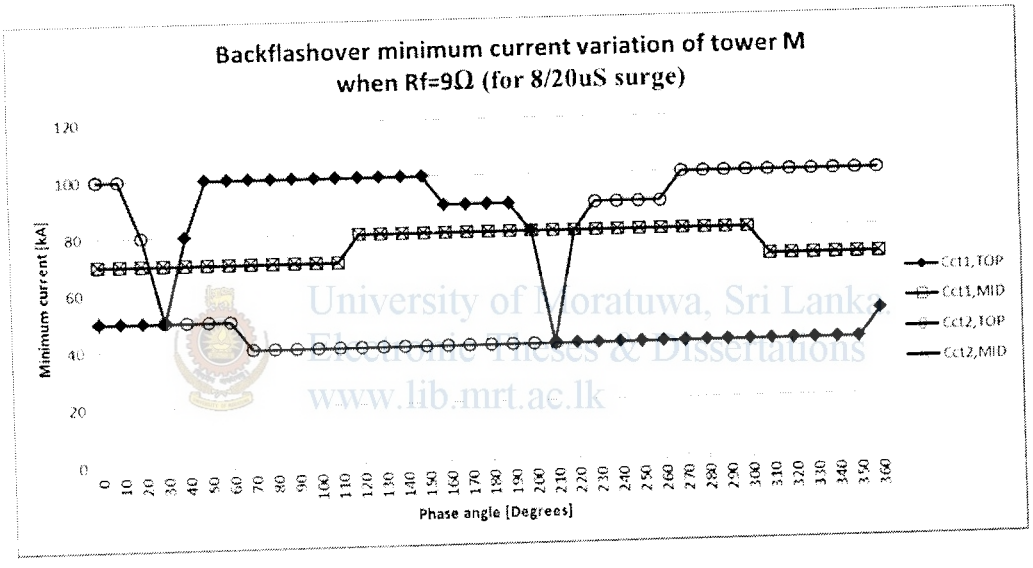

Figure 5.2 – Results of simulation no.1

also done by applying selected 9Ω, 17Ω and 62Ω tower grounding resistances values.

As per the results shown in Figure 5.2(Simulation no.01) and Figure 5.4(Simulation no.02) it can be seen clearly that the results are almost same for 8x20μs current surge for both tower grounding resistances of 9Ω and 17Ω. However the results for the 62Ω tower grounding resistance with 8x20μs current surge as shown in the Figure 5.6 (Simulation no.03) is different than the first two results.

Similarly as per the Figures 5.3(Simulation no.04), 5.5(Simulation no.05) and Figure 5.7(Simulation no.06) it can be seen a clear similarity of the results given for the 1.2x50μs surge waveform for 9Ω, 17Ω and 62Ω tower grounding resistances.

All the results from simulation no.01 to 06 except the results of simulation no.03 shows that the lowest back flashover minimum current (=40kA) is recorded in the TOP phases of the both circuits. However the TOP phase of circuit-2 was flashover at 40kA only for the phase angles ranging from 60^0 to 200^0 whereas the TOP phase of the other circuit was flashover at same 40kA current only in the phase angles ranging

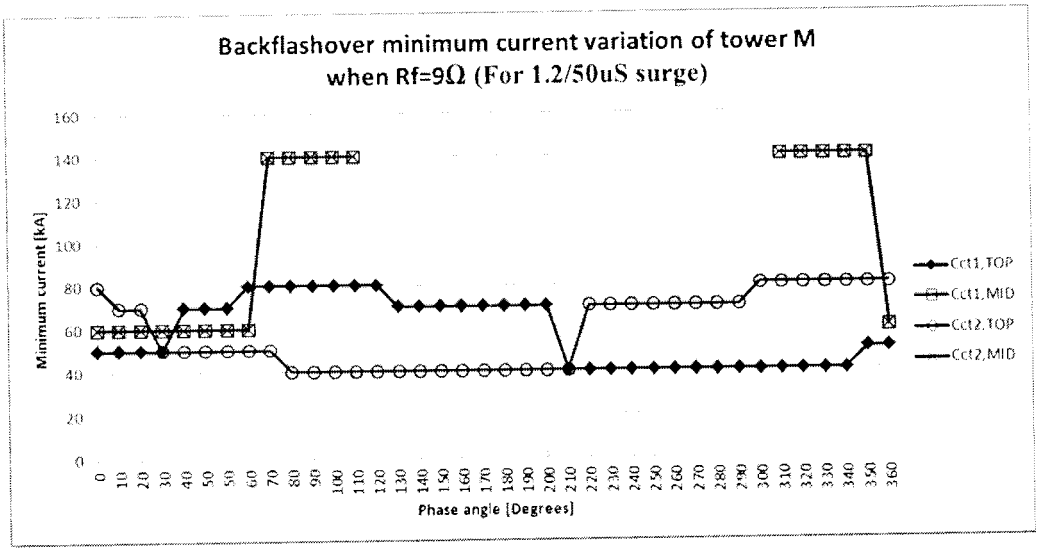

Figure 5.3 – Results of simulation no. 4

from 200^0 to 340^0. (See Figures 5.2, 5.3, 5.4, 5.5 and 5.7) Further from the above result shows that when the phase angle changes from 200^0 to 210^0 the back flash over event also changes from TOP phase of circuit-02 to TOP phase of the other circuit at 40kA surge current.

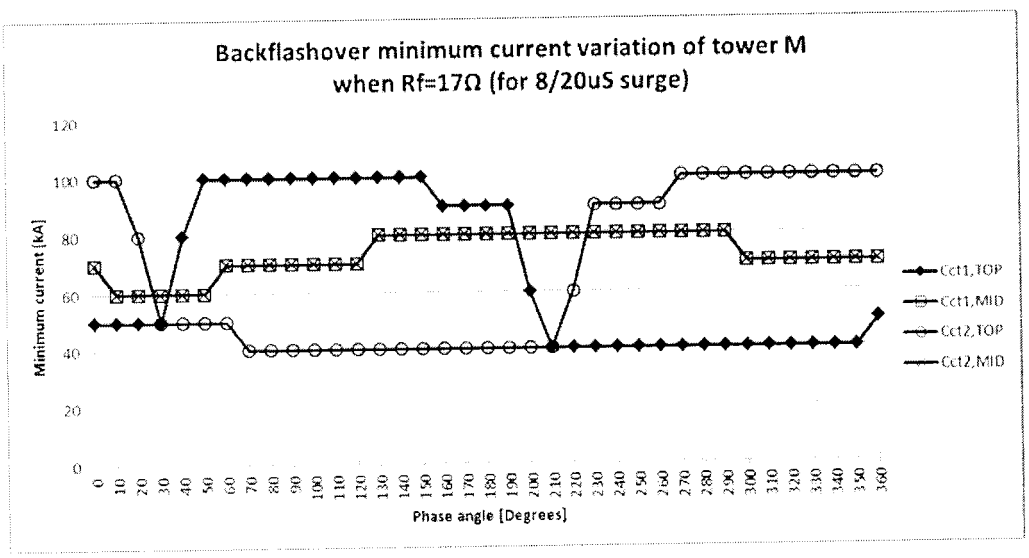

Figure 5.4 – Results of simulation no. 2

As per the results shown in the Figure 5.6 (Simulation no. 3) it shows that the MIDDLE phases and the TOP phases of both circuits are having the same lowest back flashover minimum current at 62Ω for 8x20μs surge. However the TOP phases of

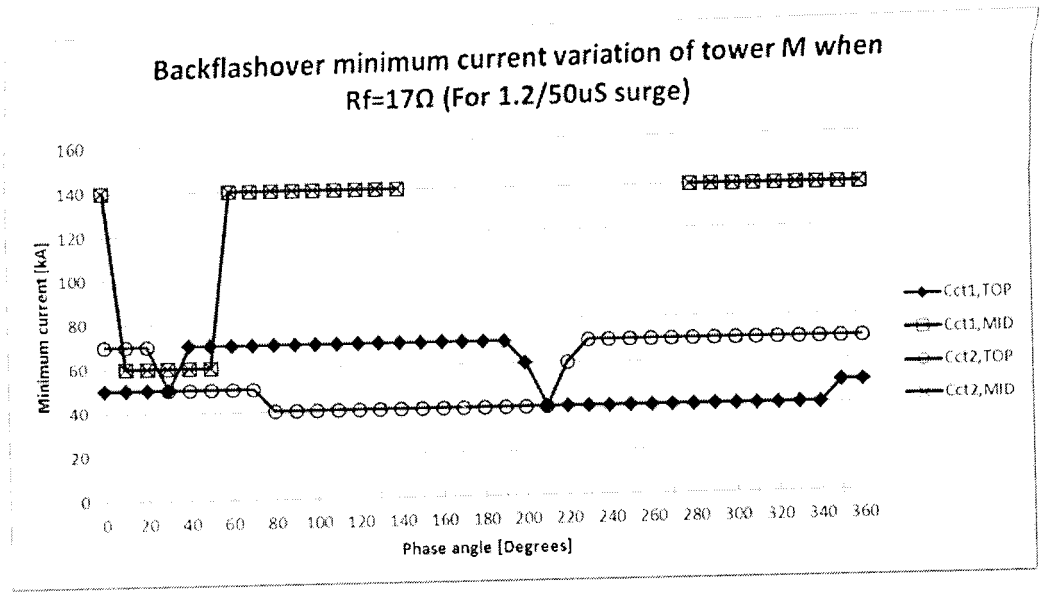

Figure 5.5 – Results of simulation no. 5

both circuits are not having the same lowest current at once at the same phase angle except at 30^0 and 210^0.

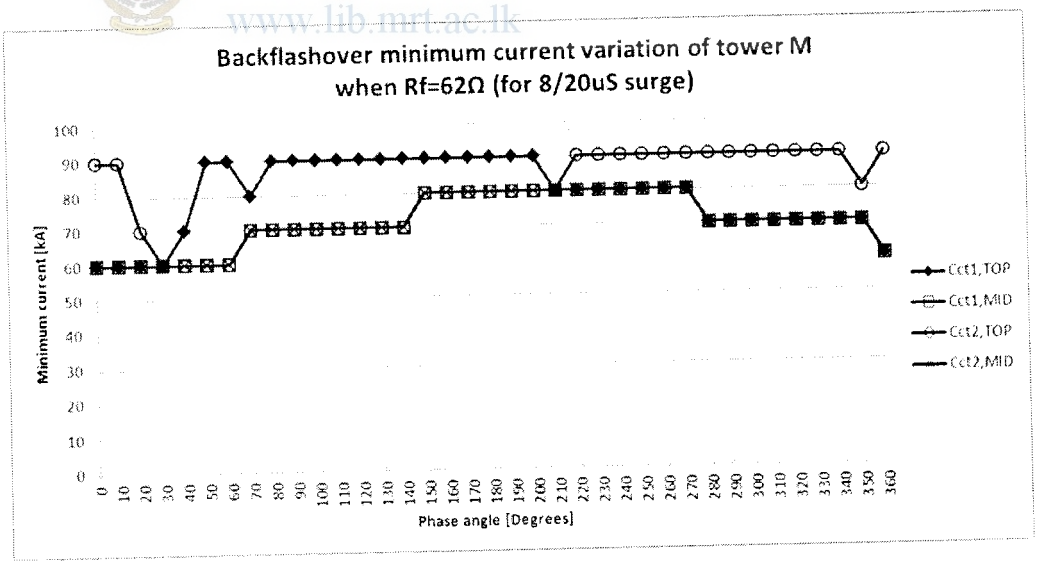

Figure 5.6 – Results of simulation no. 3

There is no back flashover events were recorded in the BOTTOM phases in any of the simulations done without arrester module. Therefore it is clear that the TOP and MIDDLE phase are more likely to have back flashovers than any of the BOTTOM phases.

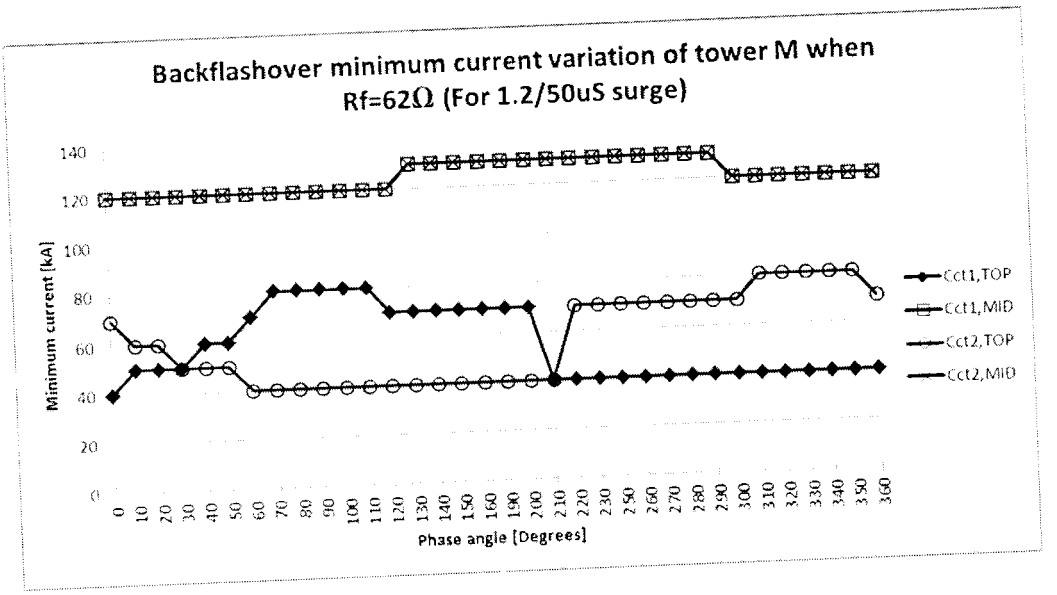

Figure 5.7 – Results of simulation no. 6

5.2.2 Results of simulations with arrester protection (Step-2)

Arrester configuration-1: Single arrester installed on TOP phase of circuit-2 of Tower-M

As per the Figures 5.8 and 5.9, the results of the simulations done with single arrester configuration are almost same for the TOP phase of circuit-01 for both 8x20µs and 1.2x50µs surge waveforms. Few back flashover events were recorded in the MIDDLE

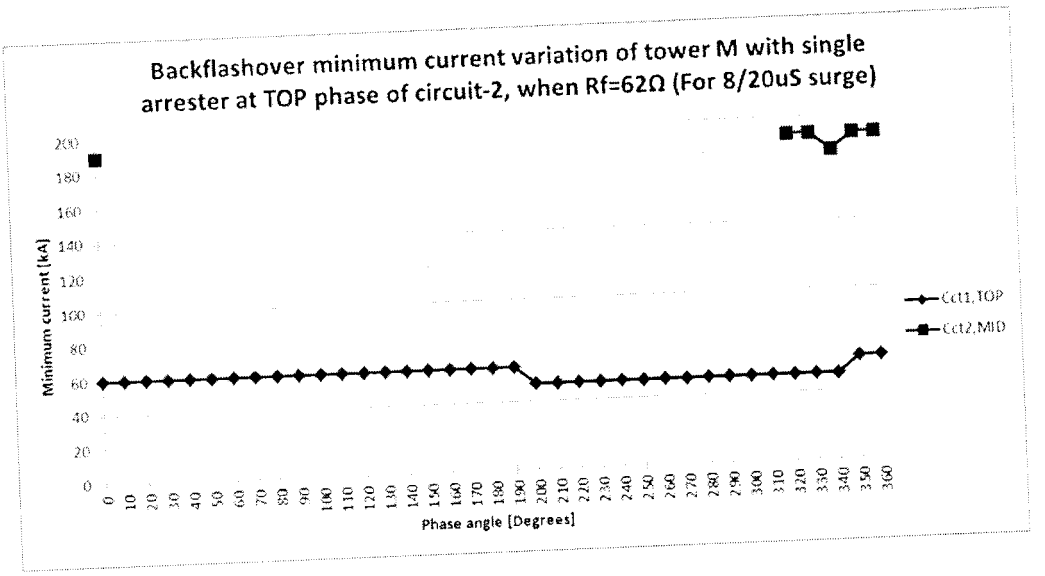

Figure 5.8 – Results of simulation no. 7

phase of the circuit 2 for only 8x20μs surge waveform at phase angle 0^0 and from 320^0 to 360^0 at 180/190kA.The lowest back flashover minimum current of the TOP phase of the circuit -01 is about 50kA when the phase angle ranging from 200^0 to 340^0.

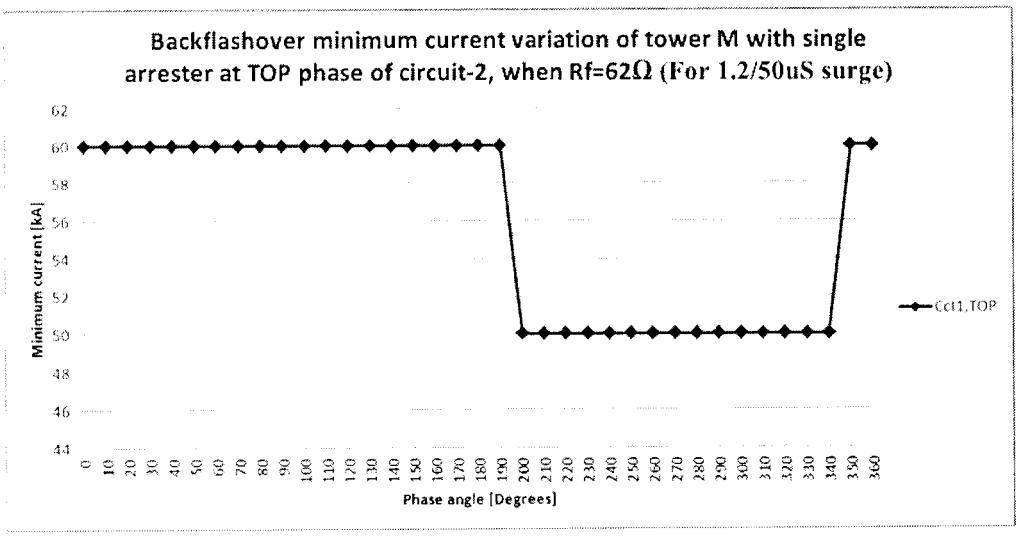

Figure 5.9 – Results of Simulation no. 8

However the back flashovers are recorded in the TOP phase of circuit-01 and the MIDDLE phase of circuit-02 only. Therefore it is clearly shows that the arrester installed in the TOP phase of the circuit-02 provides the protection against back flashovers as follows.

1. Protects the same phase (i.e. TOP phase of circuit-02) up to 200kA
2. Protects the TOP phase of circuit-01up to 50kA
3. BOTTOM and MIDDLE phases of circuit-01 up to 200kA
4. BOTTOM phase of circuit -02 up to 200kA and MIDDLE phase up to 180kA

Arrester configuration-2: Two (02) arresters each installed on TOP phase of circuit-1 and circuit-2 of Tower-M

As per the results of simulation no. 09 and 10 (with two arrester configuration), it is clearly noticed that there is no back flashovers occurs on any phase of the Tower-M

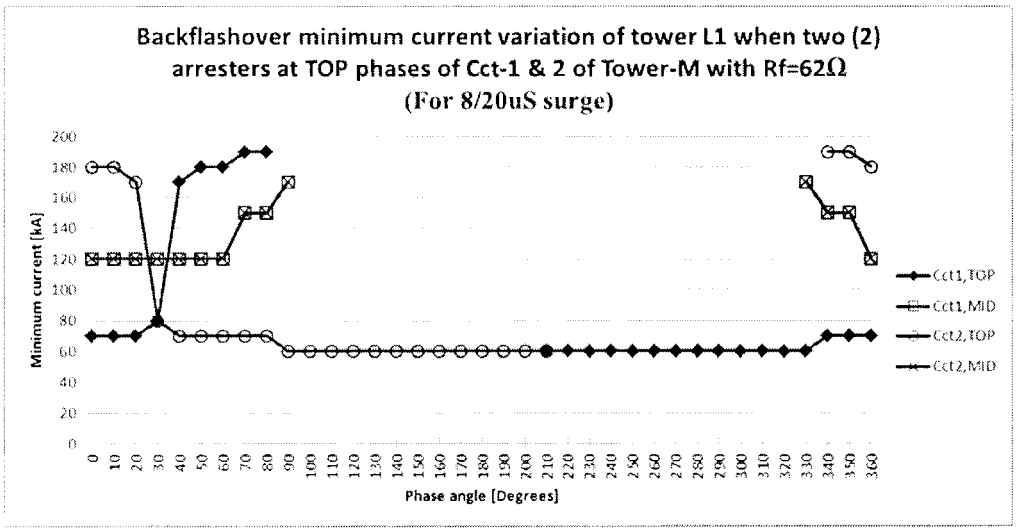

Figure 5.10 – Results of Simulation no. 11

for any of the selected three tower grounding resistance values for both surge waveforms. Therefore two arrester configuration of Tower M provides the full protection against back flashovers for all phases of the same tower.

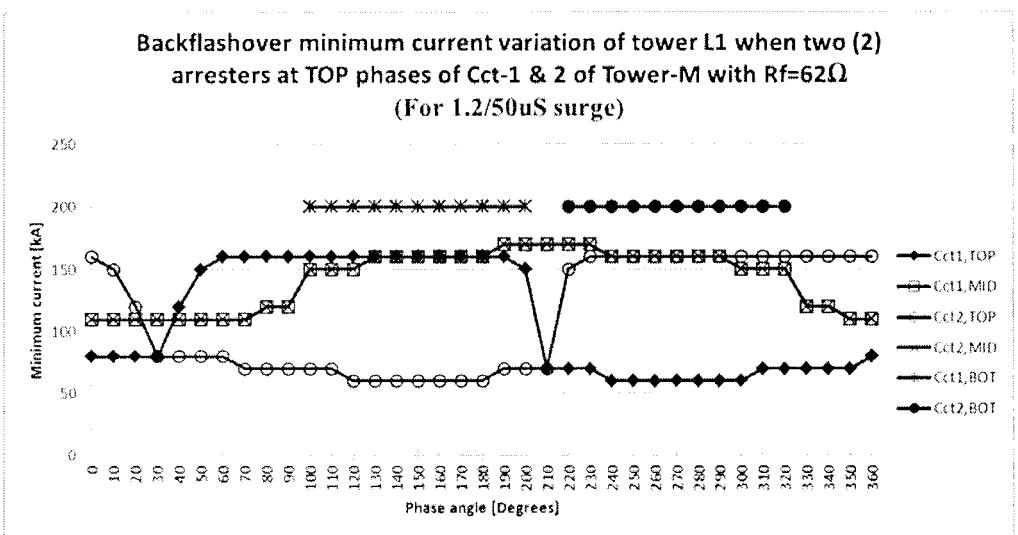

Figure 5.11 – Results of Simulation no. 12

However the results given in the Figure 5.10 and 5.11 shows that back flashover events were recorded in almost all phases of both circuits of the adjacent tower L1

even if the grounding resistance of tower M is at 62Ω for both surges. Therefore the two arrester configuration at Tower M is not providing the protection against back flashovers for the adjacent towers.